IN THE CLAIMS:

A listing of the claims follows. The claims are in the format required by 35 C.F.R. § 1.121.

1. (Original) A system comprising:

a clock source;

a first counter coupled to receive a clock signal from the clock source and configured to count cycles of the clock signal in a sample period corresponding to a first digital data stream;

a second counter coupled to receive the clock signal from the clock source and configured to count cycles of the clock signal in a sample period corresponding to a second digital data stream; and

a data processor coupled to the first and second counters and configured to

read a first number of cycles counted by the first counter and a second number of cycles counted by the second counter, and

convert at least one of the first and second digital data streams from a corresponding input sample rate to a predetermined sample rate based on the number of cycles counted in the corresponding digital data stream.

2. (Original) The system of claim 1, wherein the first counter is configured to count cycles corresponding to the first digital data stream by incrementing once for each cycle after a frame sync signal is received in the first digital data stream and wherein the second counter is configured to count cycles corresponding to the second digital data stream by incrementing once for each cycle after a frame sync signal is received in the second digital data stream.

3. (Original) The system of claim 1, further comprising a low-pass filter configured to filter the first number of cycles and the second number of cycles.

4. (Original) The system of claim 1, wherein the data processor is configured to reset the first and second counters each time a succeeding frame sync signal is received.

5. (Original) The system of claim 1, wherein the first and second digital data streams are not restricted to a set of predetermined sample rates.

6. (Original) The system of claim 1, wherein the system is implemented in a single sample rate converter.

7. (Original) The system of claim 1, wherein the data processor is configured to convert the first and second digital data streams from the corresponding input sample rates to the predetermined sample rate in corresponding channels, wherein at least a portion of a plurality of processing components of the channels are common to each of the channels.

8. (Original) The system of claim 1, wherein the data processor is configured to: estimate a primary rate for the first digital data stream based upon the cycles counted by the first counter; and to estimate a secondary rate for the second digital data stream based upon a ratio of the cycles counted by the second counter to the cycles counted by the first counter.

9. (Original) The system of claim 8, further comprising a first FIFO and a second FIFO, wherein data from the first digital data stream is stored in the first FIFO and data from the second digital data stream is stored in the second FIFO.

10. (Original) The system of claim 9, wherein the data processor is further configured to: convert the first digital data stream to the predetermined rate based on the estimated primary rate and convert the second digital data stream to the predetermined rate based on the estimated secondary rate.

11. (Original) A method comprising:
receiving a clock signal from a clock source;
receiving a first digital data stream;
receiving a second digital data stream;
counting a first number of cycles of the clock signal in a sample period corresponding to a first digital data stream and a second number of cycles of the clock signal in a sample period corresponding to a second digital data stream; and
converting at least one of the first and second digital data streams from a corresponding input sample rate to a predetermined sample rate based on the number of cycles counted for the corresponding digital data stream.

12. (Original) The method of claim 11, wherein counting the first number of cycles for the first digital data stream comprises incrementing a first counter once for each cycle after a frame sync signal is received in the first digital data stream and counting the second number of cycles for the second digital data stream comprises incrementing a second counter once for each cycle after a frame sync signal is received in the second digital data stream.

13. (Original) The method of claim 12, wherein counting the first number of cycles for the first digital data stream further comprises reading a first value from the first counter and wherein counting the second number of cycles for the second digital data stream further comprises reading a second value from the second counter.

14. (Original) The method of claim 11, further comprising resetting the first and second counters each time a succeeding frame sync signal is received.

15. (Original) The method of claim 11, further comprising estimating a primary rate for the first digital data stream based upon the first number of cycles and estimating a secondary rate for the second digital data stream based upon a ratio of the first number of cycles and the second number of cycles.

16. (Original) The method of claim 15, further comprising storing data from the first digital data stream in a first FIFO and storing data from the second digital data stream in a second FIFO.

17. (Original) The method of claim 16, further comprising converting the first digital data stream to the predetermined rate based on the estimated primary rate and converting the second digital data stream to the predetermined rate based on the estimated secondary rate.

18. (Original) The method of claim 11, further comprising low-pass filtering the first number of cycles and the second number of cycles.

19. (Original) The method of claim 11, wherein the first and second digital data streams are not restricted to a set of predetermined sample rates.

20. (Original) The method of claim 11, wherein the method is implemented in a digital audio amplifier.

21. (Original) The method of claim 20, wherein the method is implemented in a pulse-width modulated digital audio amplifier.